A 20-50GHz MMIC Amplifier with 21dBm Output Power and its Application as a Frequency Doubler

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Abstract

A 20-50GHz MMIC amplifier, designed on a 0.25μm-gate PMODFET production IC process, has demonstrated a 13 ±1.8 dB gain with greater than 21dBm saturated output power across the band. A traveling-wave-input/power-combined-output configuration developed for the input stage design has facilitated area-efficient broadband impedance matching and also enabled the amplifier to operate as a frequency doubler. More than 10dBm output power was achieved over the 20-50GHz doubled frequency band for 20dBm input power.

I. Introduction

Performance of mm-wave MMIC power amplifiers has continued to improve in gain, power and efficiency for various military and commercial applications [1]-[5]. Emerging needs for mm-wave links to support satellite communications and RF personal communication networks have further increased the importance of such amplifiers as well as measurement systems to test mm-wave components.

This paper describes the design and performance of a 20-50GHz power amplifier intended to provide reliable broadband power operation with a small chip size primarily for wideband test and measurement system applications. A unique application of the amplifier as a frequency doubler is also presented.

Section II briefly summarizes HP's 50GHz MMIC process used for the amplifier. Section III discusses the amplifier design focusing on a traveling-wave-input/power-combined-output configuration. Measured performance of the amplifier is shown in Sections IV and V.

II. 50GHz MMIC Process

The 50GHz MMIC production process, used for the amplifier design, has been developed for RF/microwave/mm-wave and high-speed circuits especially for large signal operation [6]. The active device, P-MODFET, is fabricated on an MBE-grown pseudomorphic epitaxial structure with a 150Å undoped InGaAs channel on an AlGaAs/GaAs superlattice buffer layer. Unlike a conventional P-MODFET, the device employs a GaAs carrier supply layer above the channel to improve power linearity under large signal operation [7].

A 0.25μm Ti/Pt/Au mushroom gate formed in a recess area resides 0.5μm away from a source ohmic contact to minimize source resistance. A 1000Å-thick PECVD Si_3N_4 passivates the device, which also serves as dielectric film for MIM capacitors.

Fig.1 shows an equivalent circuit of the FET. The device offers a typical f_T of 50GHz and a f_{max} of

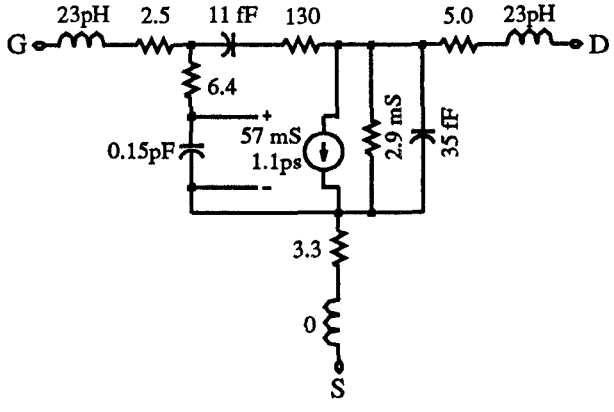

Fig. 1. An equivalent circuit of a 120μm test FET on the 50GHz MMIC process. V_{DS}=5V, I_{DS}=200mA/mm.

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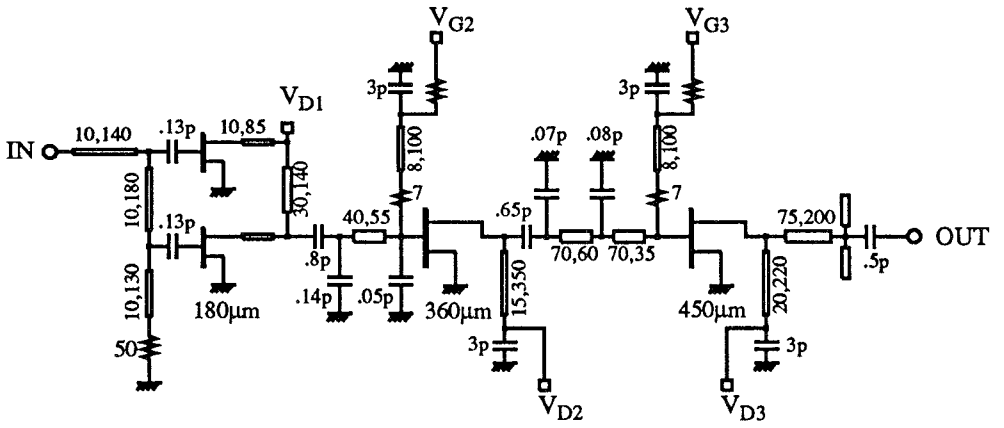

Fig. 2. Simplified circuit schematic of the 20-50GHz power amplifier.

100GHz, when biased at V_{DS}=5V and I_{DS}=200mA/mm for power operation, and delivers a 1dB-gain-compression output power of 0.4W/mm and a saturated power of 0.7W/mm at 40GHz. The device maintains high performance over a wide biasing range with >70GHz f_T achievable at lower drain voltages. A typical gate-drain breakdown voltage of 11.4V enhances device reliability under large-signal operation. The device has a MTTF of 10^6 hours at 150°C junction temperature under the typical biasing condition for power performance, with an activation energy of 1.5eV.

The MMIC process is equipped with passive components which include a 220Ω/□ n-layer bulk resistor, 22Ω/□ Ta_2N thin film resistor, 0.60fF/μm^2 Si_3N_4 MIM capacitor, 27pH backside via and two metal layers for transmission lines.

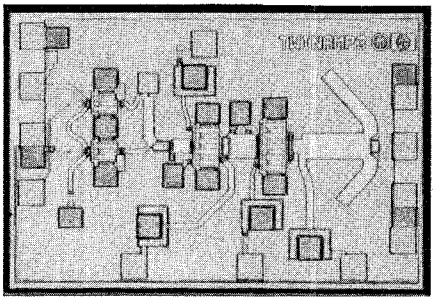

Fig. 3. Microphotograph of the 20-50GHz power amplifier. The chip measures 1.28 x 0.86 mm^2.

III. Amplifier Design

Fig. 2 shows a simplified circuit schematic of the 20-50GHz three-stage power amplifier. The amplifier is featured by the first input stage which incorporates a traveling-wave-input / power-combined-output configuration with two identical FET cells. The traveling-wave-input matched to 50 ohms greatly simplifies the design of a broadband input matching network the layout of which otherwise tends to consume a large area in a conventional power amplifier design. The power-combined-output eliminates a power loss which would result to the reverse termination in a standard traveling wave amplifier design with a small number of FET cells, while maintaining a well-behaved output impedance to facilitate matching to the second-stage 360μm FET. The output artificial transmission line interconnecting the two FET cells is designed to have a characteristic impedance equal to the resistive part of the output impedance of an FET cell, so that both cell FETs see identical load impedance. The size of the cell FETs is dictated by the bandwidth coverage and the input impedance level of the 360μm FET. A mildly lossy matching scheme is employed between the 360μm and 450μm FETs. A reactive output matching network provides the 450μm FET with optimum load impedance for maximum output power across the band. The optimum load was experimentally determined using an on-wafer load-pull measurement system [8].

Fig. 3 shows a photograph of a fabricated amplifier chip which measures 1.28 x 0.86 mm^2.

IV. Amplifier Performance

Fig. 4 exhibits the measured small-signal gain and input/output matching of the amplifier biased at V_D = 4.5V and I_D = 230mA. A gain of 13 ±1.8 dB was achieved across the 20-50GHz band with better than 7.5dB input return loss in a DC-50GHz range. The reverse isolation of the amplifier was greater than 45dB below 50GHz.

Fig. 5 plots the amplifier's power performance which was measured using an on-wafer characterization system described in reference [8]. Greater than 18dBm output power was achieved at 1dB gain compression points across the band. The saturated power well exceeds 21dBm up to 40GHz beyond which the measurement was limited by the characterization system. Although the amplifier was not designed for high efficiency, a maximum power-added efficiency of 8.0-12.0% was observed over the frequency band.

V. Performance as a Frequency Doubler

When the FETs in the first amplifier stage are biased below their pinch-off voltage, they function as an efficient second harmonic generator and thus the amplifier operates as a frequency doubler with filtered post amplification. Good input return loss of the doubler at both fundamental and second harmonic frequencies is preserved due to the traveling-wave-input configuration, as is indicated in Fig. 6. The gate voltage of the first stage was experimentally adjusted to obtain a minimum conversion loss at 50GHz output frequency while the gate voltage for the second and third stages were set exactly the same as for the amplifier operation shown in Fig. 4.

Fig. 7 shows the output power from the doubler as a function of output frequency for two levels of input power. The minimum conversion loss was observed approximately at the 15dBm input power. More than 10dBm output power was obtained over the 20-50GHz output frequency range for an input power of 20dBm.

VI. Conclusion

A 20-50GHz MMIC amplifier has been developed to demonstrate a 13 ±1.8 dB gain with greater than 21dBm saturated power. A traveling-wave-input/ power-combined-output scheme developed for the first amplifier stage has resulted in an area-efficient broadband amplifier design and also enabled the amplifier's operation as a frequency doubler.

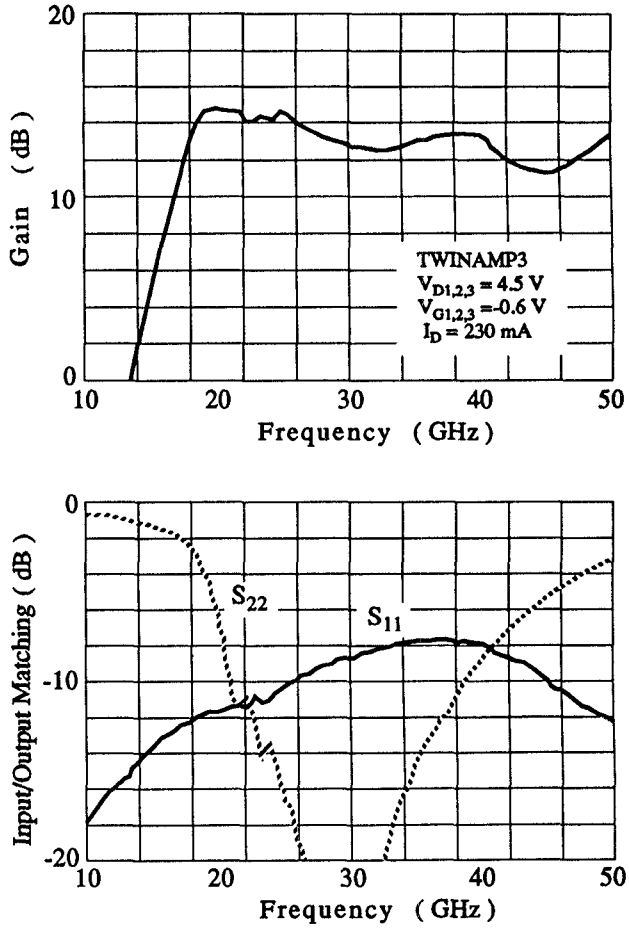

Fig. 4. Measured small-signal gain and input/output matching of the 20-50GHz power amplifier.

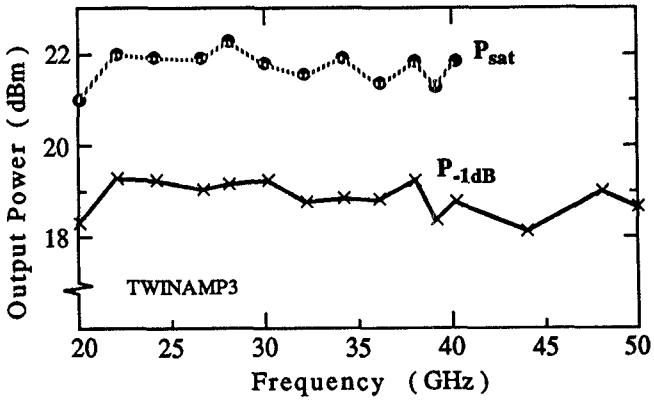

Fig. 5. Measured power performance of the 20-50GHz power amplifier.
$V_{D1,2,3}$ = 4.5 V, $V_{G1,2,3}$ =-0.6 V,
I_D = 230 mA

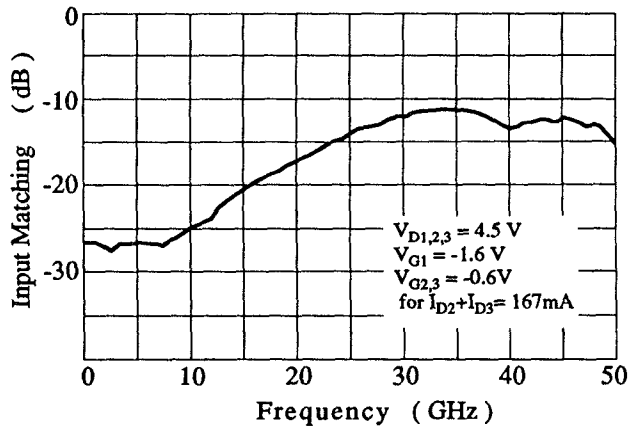

Fig. 6. Input return loss of the 20-50GHz power amplifier used as a frequency doubler.

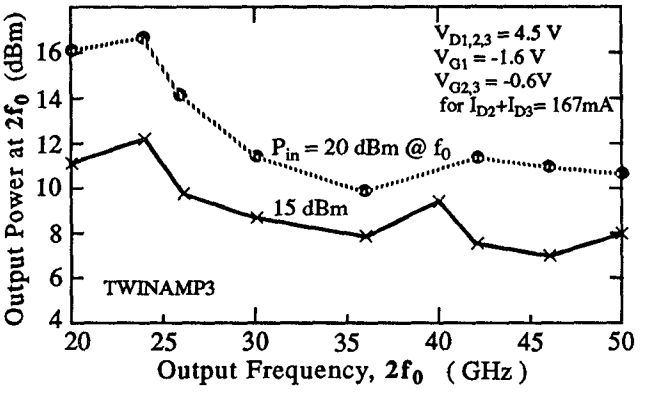

Fig. 7. Measured second harmonic power of the 20-50GHz amplifier used as a frequency doubler.

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